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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/587,237	ARAI ET AL.	
	Examiner	Art Unit	
	HAJAR KOLAHDOUZAN	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7/26/2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 July 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/20/2008 and 7/26/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-6 and 10-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamazaki et al (US 2003/0034497 A1).

Regarding claim 1, Yamazaki [figs.1-2B] teaches a semiconductor device comprising:

an integrated circuit using a thin film transistor [104a-c];

an antenna [the upper conductive bar that is connected to the TFT 104c];

a first sealing film [114]; a second sealing film [111]; and a substrate [112],

wherein the integrated circuit [104] and the antenna [the upper conductive bar that is connected to the TFT 104c] are electrically connected to each other [shown],

the integrated circuit [104] is sandwiched between [shown in fig.2B] the first sealing film [114] and the second sealing film [111],

the first sealing film [114] is sandwiched between the substrate [112] and the integrated circuit [104],

the first sealing film [114] includes a plurality of first insulating films [114a and 114c] and one or a plurality of second insulating films [114b] sandwiched between the plurality of first insulating films [shown],

the second sealing film [111] includes a plurality of third insulating films [11a and 111c] and one or a plurality of fourth insulating films [114b] sandwiched between the plurality of third insulating films [shown in fig.1C],

the one or the plurality of second insulating films [114b] has lower stress than the plurality of first insulting films [114b is a stress relaxing layer],

the one or the plurality of fourth insulating films [111b] has lower stress than the plurality of third insulating films [111b is a stress relaxing layer], and

the plurality of first insulating films [114a and 114c (the barrier layers)] and the plurality of third insulating films [111a and 111c (the barrier layers)] are inorganic insulating films [paragraph 0017].

Regarding claim 2, Yamazaki [Figs.1-2B] teaches a semiconductor device comprising:

an integrated circuit using a thin film transistor [104a-c];

an antenna [the upper conductive bar that is connected to the TFT 104c]; a first sealing film [114];

a second sealing film [111]; a substrate [112]; and a cover member [110],

wherein the integrated circuit [104] and the antenna [the upper conductive bar that is connected to the TFT 104c] are electrically connected to each other [shown],

the integrated circuit [104] is sandwiched between the first sealing film [114] and the second sealing film [111],

the first sealing film [114] and the second sealing film [111] are sandwiched between the substrate [112] and the cover member [110],

the first sealing film [114] includes a plurality of first insulating films [114a and 114c] and one or a plurality of second insulating films [114b] sandwiched between the plurality of first insulating films [shown],

the second sealing film [111] includes a plurality of third insulating films [111a and 111c] and one or a plurality of fourth insulating films [111b] sandwiched between the plurality of third insulating films [shown],

the one or the plurality of second insulating films [114b] has lower stress than the plurality of first insulating films [114b is a stress relaxing layer],

the one or the plurality of fourth insulating films [111b] has lower stress than the plurality of third insulating films [111b is a stress relaxing layer],

and the plurality of first insulating films and the plurality of third insulating films are inorganic insulating films.

Regarding claim 3, Yamazaki [figs. 1-2B] teaches a semiconductor device comprising:

an integrated circuit using a thin film transistor [104]; an antenna [the upper conductive bar that is connected to the TFT 104c];

a first sealing film [114]; a second sealing film [111]; a substrate [112]; and a cover member [110],

wherein the integrated circuit [104] and the antenna [the upper conductive bar that is connected to the TFT 104c] are electrically connected to each other [shown],

the integrated circuit [104] and the antenna [the upper conductive bar that is connected to the TFT 104c] are sandwiched between the first sealing film [114] and the second sealing film [111],

the first sealing film [114] and the second sealing film [111] are sandwiched between [shown] the substrate [112] and the cover member [110],

the first sealing film [114] includes a plurality of first insulating films [114a and 114c] and one or a plurality of second insulating films [114b] sandwiched between the plurality of first insulating films [it is shown that the layer 114b is sandwiched between 114a and 114c],

the second sealing film [111] includes a plurality of third insulating films [111a and 111c] and one or a plurality of fourth insulating films [111b] sandwiched between the plurality of third insulating films [it is shown that layer 111b is sandwiched between 111a and 111c],

the one or the plurality of second insulating films [114b] has lower stress than the plurality of first insulating films [114 is a stress relaxing layer],

the one or the plurality of fourth insulating films [111b] has lower stress than the plurality of third insulating films [111b is a stress relaxing layer], and

the plurality of first insulating films [114a and 114c (barrier layers)] and the plurality of third insulating films [111a and 111c (barrier layers)] are inorganic insulating films [paragraph 0017].

Regarding claim 4, Yamazaki [paragraph 0077] teaches that the cover member [110] has flexibility.

Regarding claim 5, The semiconductor device according to any one of claim 1 through claim 3, wherein the antenna and a gate electrode of the thin film transistor are formed by patterning a conductive film [The presence of process limitation on product claims, which product does not otherwise patentably distinguish over prior art, cannot impart patentability to the product. *In re Stephens 145 USPQ 656 (CCPA 1965).*].

Regarding claim 6, The semiconductor device according to any one of claim 1 through claim 3, wherein the antenna and a wiring connected to the thin film transistor are formed by patterning a conductive film [The presence of process limitation on product claims, which product does not otherwise patentably distinguish over prior art, cannot impart patentability to the product. *In re Stephens 145 USPQ 656 (CCPA 1965).*].

Regarding claim 10, Yamazaki [paragraph 0077] teaches that the substrate [112] has flexibility.

Regarding claim 11, Yamazaki [paragraph 0070] teaches that the plurality of first insulating films [114a and 114c] or the plurality of third insulating films [111a and 111c] includes silicon nitride, silicon nitride oxide, aluminum oxide, aluminum nitride, aluminum nitride oxide or aluminum silicon nitride oxide.

Regarding claim 12, Yamazaki [paragraph 0072] teaches that the one or the plurality of second insulating films [114b] or the one or the plurality of third insulating films [111b] includes polyimide, acrylic, polyamide, polyimide amide, benzocyclobutene or epoxy resin

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 7-8 and 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki in view of Yamazaki et al. [hereinafter Yamazaki2] (US 2002/0134979 A1).

Regarding claim 7, Yamazaki [figs.1-2B] teaches a semiconductor device comprising:

an integrated circuit using a thin film transistor [104a-c]; an antenna [the upper conductive bar that is connected to the TFT 104c]; a first sealing film [114]; a second sealing film [111]; a substrate [112]; and a cover member [110],

wherein the integrated circuit [104] is sandwiched between the first sealing film [114] and the second sealing film [111],

the first sealing film [114] and the second sealing film [111] are sandwiched between [shown] the substrate [112] and the cover member [110],

the integrated circuit and the antenna are electrically connected to each other via a contact hole formed in the cover member and the second sealing film,

the first sealing film [114] includes a plurality of first insulating films [114a and 114c] and one or a plurality of second insulating films [114b] sandwiched between the plurality of first insulating films [shown],

the second sealing film [111] includes a plurality of third insulating films [111a and 111c] and one or a plurality of fourth insulating films [111b] sandwiched between the plurality of third insulating films [shown],

the one or the plurality of second insulating films [114b] has lower stress than the plurality of first insulating films [114b is a stress relaxing layer],

the one or the plurality of fourth insulating films [111b] has lower stress than the plurality of third insulating films [111b is a stress relaxing layer], and

the plurality of first insulating films [114a and 114c] and the plurality of third insulating films [111a and 111c] are inorganic insulating films [paragraph 0017].

But Yamazaki does not disclose that the cover member [110] is sandwiched between the antenna and the second sealing film,

However, Yamazaki2 [Fig.1] teaches a semiconductor component that has TFTs and antenna and cover member and it further teaches that the cover member [39] is sandwiched between the antenna [44] and the second sealing film [12]. Therefore it would have been obvious to one ordinary skill in the art at the time of the invention to place the cover member between the antenna and the second sealing film because with this structure the antenna would have contact to the outside and other circuits.

Regarding claim 8, Yamazaki in view of Yamazaki2 was discussed in claim 7. Yamazaki [paragraph 0077] teaches that the cover member [110] has flexibility.

Regarding claim 10, Yamazaki in view of Yamazaki2 was discussed in claim 7. Yamazaki [paragraph 0077] teaches that the substrate [112] has flexibility.

Regarding claim 11, Yamazaki in view of Yamazaki2 was discussed in claim 7. Yamazaki [paragraph 0070] teaches that the plurality of first insulating films [114a and 114c] or the plurality of third insulating films [111a and 111c] includes silicon nitride, silicon nitride oxide, aluminum oxide, aluminum nitride, aluminum nitride oxide or aluminum silicon nitride oxide.

Regarding claim 12, Yamazaki in view of Yamazaki2 was discussed in claim 7. Yamazaki [paragraph 0072] teaches that the one or the plurality of second insulating films [114b] or the one or the plurality of third insulating films [111b] includes polyimide, acrylic, polyamide, polyimide amide, benzocyclobutene or epoxy resin

5. Claims 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki in view of Tanaka et al. (US 6,974,909 B2).

Regarding claim 9, Yamazaki [Figs.1-2B] teaches a semiconductor device comprising:

an integrated circuit using a thin film transistor [104a-c];

a first sealing film [114] ; a second sealing film [111]; and a substrate [112],

wherein the integrated circuit [104] is sandwiched between the first sealing film [114] and the second sealing film [111], the first sealing film [114] is sandwiched between the substrate [112] and the integrated circuit [104].

the integrated circuit [104] includes a connection terminal [terminals are shown in Fig.1B but are not labeled],

the first sealing film [114] includes a plurality of first insulating films [114a and 114c] and one or a plurality of second insulating films [114b] sandwiched between the plurality of first insulating films [shown],

the second sealing film [111] includes a plurality of third insulating films [111a and 111c] and one or a plurality of fourth insulating films [111b] sandwiched between the plurality of third insulating films [shown],

the one or the plurality of second insulating films [114b] has lower stress than the plurality of first insulating films [114b is a stress relaxing layer],

the one or the plurality of fourth insulating films [111b] has lower stress than the plurality of third insulating films [111b is a stress relaxing layer], and

the plurality of first insulating films [114a and 114c] and the plurality of third insulating films [111a and 111c] are inorganic insulating films [paragraph 0017].

But Yamazaki does not disclose that the integrated circuit further includes a rectification circuit for generating a supply voltage from an alternating-current signal that is input in the connection terminal by an antenna;

a demodulation circuit for generating a first signal by demodulating the alternating-current signal; a microprocessor for performing arithmetic processing in accordance with the first signal to generate a second signal; a modulation circuit for modulating the second signal; and a switch for modulating load applied to the antenna in accordance with the modulated second signal.

Tanaka [Fig.7] teaches an integrated circuit that includes a rectification circuit [121] for generating a supply voltage from an alternating-current signal that is input in the connection terminal by an antenna [100];

a demodulation circuit [123] for generating a first signal by demodulating the alternating-current signal; a microprocessor [126] for performing arithmetic processing in accordance with the first signal to generate a second signal; a modulation circuit [circuit 20 that modulates a carrier wave] for modulating the second signal; and a switch for modulating load applied to the antenna in accordance with the modulated second signal [shown].

Therefore it would have been obvious to one ordinary skill in the art at the time of the invention to have associated the semiconductor component of Yamazaki with the circuit of Tanaka which includes rectifier, modulator/demodulator, microprocessor, and switch to control

the voltage given to the TFTs by converting high voltage to low voltage and to make the semiconductor function.

Regarding claim 10, Yamazaki in view of Tanaka was discussed in claim 9. Yamazaki [paragraph 0077] teaches that the substrate [112] has flexibility.

Regarding claim 11, Yamazaki in view of Tanaka was discussed in claim 9. Yamazaki [paragraph 0070] teaches that the plurality of first insulating films [114a and 114c] or the plurality of third insulating films [111a and 111c] includes silicon nitride, silicon nitride oxide, aluminum oxide, aluminum nitride, aluminum nitride oxide or aluminum silicon nitride oxide.

Regarding claim 12, Yamazaki in view of Tanaka was discussed in claim 9. Yamazaki [paragraph 0072] teaches that the one or the plurality of second insulating films [114b] or the one or the plurality of third insulating films [111b] includes polyimide, acrylic, polyamide, polyimide amide, benzocyclobutene or epoxy resin

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HAJAR KOLAHDOUZAN whose telephone number is (571)270-5842. The examiner can normally be reached on Monday- Friday 7:30 A.M.- 5:00 P.M. EDT.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne Monbleau can be reached on (571) 272-1945. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HK

/Davienne Monbleau/
Supervisory Patent Examiner, Art Unit 2893